Unlocking RISC-V’s potential with Custom Compute

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Future of Computing Day 2024
→ Codasip overview

• Founded in 2014
• HQ in Munich
• ~250 employees
• Design teams in Europe
• Processor solution company
• RISC-V co-founder
• Enabling Custom Compute
→ All failing: 
Moore’s law, Dennard scaling, Amdahl’s law

• After 50 years of driving semiconductor economics, underlying “semiconductor laws” are failing
• At the same time, everything is getting prohibitively expensive

Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e. 2018
→ Only really one option near-term

Customize hardware to workload

(*heterogeneous compute/domain specific acceleration*)
This is what Codasip does...

Transforming how the world designs microprocessors

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**Codasip**

CodAL

+ 

**Codasip**

Studio

+ 

RISC-V: The Free and Open RISC Instruction Set Architecture

C-based language

Design tool

Open ISA
RISC-V

- Open standard
- Modular Instruction Set Architecture
- Tailor an architecture or microarchitecture to a workload
- Allows different implementations
  - Embedded vs. application
  - Standard vs. non-standard extensions
  - Open source vs. proprietary, etc.

| Base integer | Optional standard extensions | Non-standard extensions |
Codasip Architectural Language (CodAL)
Specialized for processor design

C-like programming language with high-level processor architecture constructs and support for automation

/* Multiply and accumulate: semantics
   dst += src1 * src2 */

element i_mac {
    use reg as dst, src1, src2;
    assembly { "mac" dst "," src1 "," src2 };
    binary { OP_MAC dst src1 src2 @:bit[9] };
    semantics {
        rf[dst] += rf[src1] * rf[src2];
    }
};
→ Codasip Studio
An automated approach to custom compute
Customization optimizes your results

- Improved Performance (for a given set of applications)
- Adding custom instructions
- Adding RISC-V extensions
- Processors with custom instructions dedicated to a target application
- Processors with RISC-V extensions

Base RISC-V processor
→ Value of customization

FIR filtering profiling

- Runtime reduction >96%
- Energy consumption reduction >90%
- For +36% silicon area
  → Max frequency not affected
  → Performance gain >32x
Introducing CHERI
→ CHERI
(Capability Hardware Enhanced RISC Instructions)

Fine-grained memory protection

Revisits fundamental design choices in hardware and software to dramatically improve system security

Extend conventional hardware ISAs

• Memory protection
• Scalable compartmentalization
A security market innovation

Codasip brings 10,000 people years of R&D to the mass market with the first deployable CPUs and commercially supported offering.

- Small performance hit for CHERI code on area footprint – around 5%
- Capabilities Limited (UK) in a study compiled 6 million lines of C/C++ code for memory safety – 0.026% lines of codes needed to be modified

https://www.capabilitieslimited.co.uk/_files/ugd/f4d681_e0f23245dace466297f20a0dbd22d371.pdf
Functional Safety certification
Certification for functional safety and cybersecurity

February: IP hardware development process certified according to ISO 26262 and ISO/SAE 21434

April: First ISO 26262 product certification for L31AS
Summary

1. Semiconductor “laws” are failing
2. Custom compute provides an extraordinary opportunity to differentiate
3. Codasip’s unique approach...
   1. ... leverages RISC-V open standards
   2. ... provides architectural ownership
   3. ... delivers differentiated results
Thank you!