

Leadership in the new computing era

Future of Computing: RISC-V TUM Labs, 23.4.2024, Munich

SiFive Dr. Manfred Schlett Senior Director, Business Development manfred.schlett@sifive.com





Founded by the inventors of RISC-V



- SiFive founded 2015
- SiFive is the RISC-V founder & brand standard
- Largest team & investment
- World's largest technology companies work with SiFive to adopt RISC-V



2 Billion

Chips based on SiFive RISC-V cores















RISC-V Software Ecosystem





The success of RISC-V is built on open standards Open architecture driving exponential growth Android on RISC-V is a first-class citizen SiFive is the biggest contributor of RISC-V software tools and OS RISE consortium accelerates software optimizations on RISC-V



SiFive HiFive Premier P550 sets a new standard





- Quad-core out-of-order SiFive P550 @1.4GHz
- 4MB L3 cache, 16GB LPDDR5 (optional 32GB version)
- NPU and 2D/3D GPU
- On-board 128GB eMMC
- PCI Express Gen3 x4 via a PCIe x16 slot
- SATA3 connector (6 Gb/s)
- Dual 10/100/1000 Ethernet + remote board management ethernet port
- 5x USB 3.2 Gen1
- New System-On-Module approach (SOM)
- Mini-DTX form factor (8" x 6.7" / 203mm x 170mm)
- Ubuntu to be fully supported
- Shipping expected in July 2024 from Arrow Electronics
 - HF106-000 (16GB LPDDR5): ~ \$650
 - HF106-100 (32GB LPDDR5): ~ \$800

ANN 🗘 ubuntu

SiFive P550 Application Processor



High-Performance Out-of-Order RISC-V Application Processor



P550 Core Architectural Features

- RV64GBC capable core with Sv39/Sv48
 Virtual Memory Support
- Triple-issue, 13-stage out-of-order processor tuned for scalable performance
- Private L2 Caches for improved memory performance
- SECDED ECC with Error Reporting
- Performance 8.7 SpecINT2k6/GHz

The Undisputed Leader in RISC-V Computing



Broadest portfolio of processors from embedded to high-performance computing

CPU Cores		Al Cores	Functional Safety
Gervice Essential™	SiFive Performance™	SiFive Intelligence™	SiFive Automotive™
32 and 64-bit Processors	64-bit Application Processors	Scalable 64-bit Al Processors	32/64-bit Safety Processors
Microcontrollers, IoT devices, real-time control, control plane processing Highly customizable to application specific requirements Mature, industry proven designs	 Consumer High performance RISC-V processor with best compute density and power efficiency Android ready Infrastructure Highest performance, most advanced RISC-V processor Scale out, high performance, processing capabilities with 	 Edge Al, Cloud, Training, Inference Very high performance and efficiency for Al workloads with vector processing Built on top of RISC-V Vectors, SiFive Intelligence Extensions and Al hardware accelerators 	 Broadest range of RISC-V safety processors, from MCU to high performance SoC, with ASIL B and ASIL D options Multi-core/cluster, vectors, virtualization, and security features Strong automotive RISC-V ecosystem
	vector compute, NoC and D2D		

SiFive broad IP portfolio

Scalable from MCU to high-performance compute



SiFive

RISC-V is based on standards

Standards Accelerate Software Adoption and Portability

Standards reduce cost

- Faster Adoption
- Compatibility across vendors

Layered standards enable customization

 RISC-V embraces customization without breaking compatibility

More than just ISA Standards

 RISC-V Standards extend beyond the Core ISA to system-level components





SiFive Performance family relentless innovation





P870 Pipeline

Branch Predict/Fetch Decode/Rename







Cluster topology with shared L2 cache and distributed L3 cache





P870-A Functional safety features





Significant Area Advantage



Enabling unparalleled cost efficiency across the SiFive Performance family



Area is for Core plus private caches needed to achieve the indicated SPEC score P470 and P670 FMax measured at 0.95V and reach 2.9GHz P870 FMax measured at 0.95V and reach 3.3GHz Cortex-A55 Source: Measured on Snapdragon 7c Cortex-A76 Source: https://www.anandtech.com/shaw/13614/arm-delivers-on-cortex-a76-promises

Cortex-A78 Source: https://www.anandtech.com/show/158/3/arm-cortex-a78-cortex-x1-cpu-ip-diverging/4 TechInsights Microprocessor Reports: Die Photos Show Cortex-A78 Shortfall

Cortex-A710 and X2 Performance Estimated from:

ps://www.anandtech.com/show/16693/arm-announces-mobile-armv9-cpu-microarchitectures-cortexx2-cortexa710-cortexa5

Cortex-A710 and X2 Area from: TechInsights Microprocessor Reports MediaTek Delivers Efficient Cortex-X2:

SiFive solutions for Automotive ADAS





- Safety features including split-lock, RAS and memory safety
- Support for mixed criticality supporting ASIL-B and/or ASIL-D
- Leading compute density
- Automotive-grade software ecosystem



Component Level Construction



Modular Design for Datacenter and Automotive

Key features are high core count, scalability, and reliability

- Architected to provide a scalability path for expansion both on die and D2D
- Core disable for compute on demand and yield recovery purposes
- Larger granularity on DVFS and power gating boundaries
 - Modular architecture (tile DVFS, cluster DVFS, quadrant DVFS, etc.)
- Additional RAS features for both datacenter and automotive

Modular compilation and stampability to simplify floorplan

• Maintaining low latency while covering long distances is the goal of NoCLink



SiFive is empowering the new computing era





SiFive Software Products





- C Runtime
- CSR / MMIO + drivers
- FreeRTOS kernel
- Example programs
- Industry standard benchmarks

Embedded Linux software

- Yocto / OpenEmbedded based
- Includes U-Boot and OpenSBI
- Virtualization (AIA, IOMMU, KVM) •
- Enhanced perf support
- Enhancement kernel for IP
- Power management support •

Simulation models

- Cycle model
- Fast functional model
- SystemC interface
- TLM 2.0 interface
- Single or Multi-threaded

Empowering innovators

www.sifive.com