Leadership in the new computing era

Future of Computing: RISC-V
TUM Labs, 23.4.2024, Munich

SiFive
Dr. Manfred Schlett
Senior Director, Business Development
manfred.schlett@sifive.com
Founded by the inventors of RISC-V

- SiFive founded 2015
- SiFive is the RISC-V founder & brand standard
- Largest team & investment
- World’s largest technology companies work with SiFive to adopt RISC-V
2 Billion
Chips based on SiFive RISC-V cores
The success of RISC-V is built on open standards

Open architecture driving exponential growth

Android on RISC-V is a first-class citizen

SiFive is the biggest contributor of RISC-V software tools and OS

RISE consortium accelerates software optimizations on RISC-V
SiFive HiFive Premier P550 sets a new standard

- Quad-core out-of-order SiFive P550 @1.4GHz
- 4MB L3 cache, 16GB LPDDR5 (optional 32GB version)
- NPU and 2D/3D GPU
- On-board 128GB eMMC
- PCI Express Gen3 x4 via a PCIe x16 slot
- SATA3 connector (6 Gb/s)
- Dual 10/100/1000 Ethernet + remote board management ethernet port
- 5x USB 3.2 Gen1
- New System-On-Module approach (SOM)
- Mini-DTX form factor (8" x 6.7" / 203mm x 170mm)
- Ubuntu to be fully supported
- Shipping expected in July 2024 from Arrow Electronics
  - HF106-000 (16GB LPDDR5): ~ $650
  - HF106-100 (32GB LPDDR5): ~ $800
SiFive P550 Application Processor
High-Performance Out-of-Order RISC-V Application Processor

P550 Core Architectural Features

- RV64GBC capable core with Sv39/Sv48 Virtual Memory Support
- Triple-issue, 13-stage out-of-order processor tuned for scalable performance
- Private L2 Caches for improved memory performance
- SECDED ECC with Error Reporting
- Performance 8.7 SpecINT2k6/GHz

©2024 SiFive
The Undisputed Leader in RISC-V Computing

Broadest portfolio of processors from embedded to high-performance computing

### CPU Cores

**SiFive Essential™**
- **32 and 64-bit Processors**
  - Microcontrollers, IoT devices, real-time control, control plane processing
  - Highly customizable to application specific requirements
  - Mature, industry proven designs

**SiFive Performance™**
- **64-bit Application Processors Consumer**
  - High performance RISC-V processor with best compute density and power efficiency
  - Android ready

**SiFive Intelligence™**
- **Scalable 64-bit AI Processors**
  - Edge AI, Cloud, Training, Inference
  - Very high performance and efficiency for AI workloads with vector processing
  - Built on top of RISC-V Vectors, SiFive Intelligence Extensions and AI hardware accelerators

### AI Cores

### Functional Safety

**SiFive Automotive™**
- **32/64-bit Safety Processors**
  - Broadest range of RISC-V safety processors, from MCU to high performance SoC, with ASIL B and ASIL D options
  - Multi-core/cluster, vectors, virtualization, and security features
  - Strong automotive RISC-V ecosystem
# SiFive broad IP portfolio

Scalable from MCU to high-performance compute

<table>
<thead>
<tr>
<th><strong>Intelligence</strong></th>
<th><strong>Performance</strong></th>
<th><strong>Automotive</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>X200-Series</strong></td>
<td><strong>P200-Series</strong></td>
<td><strong>E6-Series</strong></td>
</tr>
<tr>
<td>512-bit VLEN</td>
<td>2-wide in-order core</td>
<td>32-bit, balanced performance and efficiency</td>
</tr>
<tr>
<td>Single Vector ALU</td>
<td>256b vector length</td>
<td>ASIL B, D</td>
</tr>
<tr>
<td>VCIX</td>
<td>WorldGuard</td>
<td></td>
</tr>
<tr>
<td><strong>X300-Series</strong></td>
<td><strong>P400-Series</strong></td>
<td><strong>S7-Series</strong></td>
</tr>
<tr>
<td>Up to 1024-bit VLEN</td>
<td>3-wide OoO core</td>
<td>64-bit, high performance</td>
</tr>
<tr>
<td>Single / Dual Vector ALU</td>
<td>128b vector length</td>
<td>embedded ASIL D</td>
</tr>
<tr>
<td>VCIX</td>
<td>Hypervisor extension</td>
<td></td>
</tr>
<tr>
<td></td>
<td>WorldGuard</td>
<td><strong>X280-Series</strong></td>
</tr>
<tr>
<td></td>
<td>RVA20</td>
<td>512-bit VLEN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single Vector ALU</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCIX</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Essential</strong></th>
<th><strong>P500-Series</strong></th>
<th><strong>S6-Series</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>U6-Series</strong></td>
<td>64-bit, high performance</td>
<td>64-bit, high performance</td>
</tr>
<tr>
<td><strong>U7-Series</strong></td>
<td>64-bit, superscalar performance</td>
<td>embedded ASIL D</td>
</tr>
<tr>
<td><strong>S2-Series</strong></td>
<td>64-bit, Area optimized</td>
<td></td>
</tr>
<tr>
<td><strong>S6-Series</strong></td>
<td>64-bit, power efficiency</td>
<td></td>
</tr>
<tr>
<td><strong>S7-Series</strong></td>
<td>64-bit, high performance, embedded</td>
<td></td>
</tr>
<tr>
<td><strong>E2-Series</strong></td>
<td>Smallest, most efficient</td>
<td></td>
</tr>
<tr>
<td><strong>E6-Series</strong></td>
<td>Balanced performance and efficiency</td>
<td></td>
</tr>
<tr>
<td><strong>E7-Series</strong></td>
<td>32-bit, optimized performance</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Automotive</strong></th>
<th><strong>P600-Series</strong></th>
<th><strong>E6-Series</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>U6-Series</strong></td>
<td>6-wide OoO core</td>
<td>32-bit, balanced performance and efficiency</td>
</tr>
<tr>
<td><strong>U7-Series</strong></td>
<td>128b vector length</td>
<td>ASIL B, D</td>
</tr>
<tr>
<td><strong>P280-Series</strong></td>
<td>Hypervisor extension</td>
<td></td>
</tr>
<tr>
<td><strong>P200-Series</strong></td>
<td>WorldGuard</td>
<td></td>
</tr>
<tr>
<td><strong>P400-Series</strong></td>
<td>RVA20</td>
<td></td>
</tr>
<tr>
<td><strong>P500-Series</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>P600-Series</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>P800-Series</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RISC-V is based on standards
Standards Accelerate Software Adoption and Portability

Standards reduce cost
• Faster Adoption
• Compatibility across vendors

Layered standards enable customization
• RISC-V embraces customization without breaking compatibility

More than just ISA Standards
• RISC-V Standards extend beyond the Core ISA to system-level components
SiFive Performance family relentless innovation

- P550
- P650/P670
- P450/P470
- P870
- P870-A

More performance
Higher core count
Leading RISC-V feature deployment

Automotive specific features

3rd generation OoO core
P870 Pipeline

**Branch Predict/Fetch**
- ZBP
- I$ (Instruction Cache)
- BP2

**Decode/Rename**
- Dec (Decode)
- Ren (Rename)
- Dis (Dispatch)

**Integer**
- Iss (Issue)
- RR (Register Renaming)
- Ex (Execute)
- WB (Write Back)

**Load/Store**
- Iss
- RR
- Agen (Address Generation)
- Tag (Tagging)
- D$ (Data Cache)
- Drv (Dispatching)
- WB

**Floating Point**
- Iss
- RR
- Ex1
- Ex2
- Ex3
- Ex4
- WB

**Vector**
- Seq (Sequential)
- Ren (Rename)
- Dis (Dispatch)
- Iss (Issue)
- RR (Register Renaming)
- Ex1
- Ex2
- Ex3
- Ex4
- Ex5
- Ex6
- WB
Cluster topology with shared L2 cache and distributed L3 cache

Legend:
- LSU - Load/Store Unit
- IEX - Integer Execution Unit
- FEX - Floating Point Execution Unit
- VEX - Vector Execution Unit
- IFU - Instruction Fetch Unit
- RDU - Rename/Dispatch Unit

P870 4-core cluster
**P870-A Functional safety features**

- **Advanced RAS architecture enabling error configuration, reporting, reaction and injection**
- **Multi-Cluster Coherent Crossbar**
  - Online diagnostic and STL
  - SECDED ECC
  - High integrity L2/L3 cache controllers and SECDED ECC
- **Core Cluster 0**
  - Core pairs in lockstep
  - ASIL C
  - CPU Tile 0
  - L1 I$
  - L1 D$
  - L2$ slice 0
  - L2$ slice 1
  - Coherent Cluster bus
  - L3$ slice 0
  - L3$ slice 1
  - Memory Ports
- **Core Cluster 1**
  - ASIL D
  - CPU Tile 3
  - CPU Tile 2
  - CPU Tile 1
  - CPU Tile 0
  - L1 I$
  - L1 D$
  - L2$ slice 0
  - L2$ slice 1
  - Coherent Cluster bus
  - L3$ slice 0
  - L3$ slice 1
  - Cluster bus and crossbar with error detection code and error handling
  - High integrity interrupt controller
- **Multi-Cluster Coherent Crossbar**
- **Multi-Cluster Non-Coherent Crossbar**
- **Cluster bus and crossbar with error detection code and error handling**
- **High integrity interrupt controller**

---

**ASIL B**

**Debug**

**Interrupt**

**System, Peripheral, Front ports**

---

**SECDED ECC**

---

**L1 I$**

---

**L1 D$**

---

**L2$ slice 0**

---

**L2$ slice 1**

---

**L3$ slice 0**

---

**L3$ slice 1**

---

**ASIL C**

---

**ASIL B**
Significant Area Advantage

Enabling unparalleled cost efficiency across the SiFive Performance family

Area is for Core plus private caches needed to achieve the indicated SPEC score

- P470 and P670 FMax measured at 0.95V and reach 2.9GHz
- P870 FMax measured at 0.95V and reach 3.3GHz

Cortex-A55 Source: Measured on Snapdragon 7c

Cortex-A76 Source: https://www.anandtech.com/show/13614/arm-delivers-on-cortex-a76-promises

Cortex-A78 Source: https://www.anandtech.com/show/15813/arm-cortex-a78-cortex-x1-cpu-ip-diverging/4

TechInsights Microprocessor Reports: Die Photos Show Cortex-A78 Shortfall
Cortex-A710 and X2 Performance Estimated from:


Cortex-A710 and X2 Area from:

TechInsights Microprocessor Reports MediaTek Delivers Efficient Cortex-X2:
SiFive solutions for **Automotive ADAS**

- Safety features including split-lock, RAS and memory safety
- Support for mixed criticality supporting ASIL-B and/or ASIL-D
- Leading compute density
- Automotive-grade software ecosystem
Component Level Construction

Modular Design for Datacenter and Automotive

Key features are high core count, scalability, and reliability

- Architected to provide a scalability path for expansion both on die and D2D
- Core disable for compute on demand and yield recovery purposes
- Larger granularity on DVFS and power gating boundaries
  - Modular architecture (tile DVFS, cluster DVFS, quadrant DVFS, etc.)
- Additional RAS features for both datacenter and automotive

Modular compilation and stampability to simplify floorplan

- Maintaining low latency while covering long distances is the goal of NoCLink
SiFive is empowering the **new computing era**

Large-scale high-performance general-purpose CPU

- SiFive Performance Family
  - P470
  - P670
  - P870

High-performance NPU

- SiFive Intelligence Family
  - Vector CPU
  - Built-in AI hardware engine
  - X3M
  - X280
  - X390

or

- SiFive Intelligence Family
  - Vector CPU
  - Customer AI hardware engine
## SiFive Software Products

### Freedom Studio

**Eclipse C/C++ environment**
- Import, Edit, Build, Run
- Visual debug and trace support
- Profiling annotations
- Pipeline visualization
- Performance analyzers

### Freedom Tools

**RISC-V development tools**
- GCC + LLVM Toolsuite
- SiFive Recode
- Auto vectorization
- Configurable QEMU
- Trace decoder

### Kernel Library

**Performance libraries**
- Linear algebra
- Nonlinear functions
- Signal processing
- Neural network
- Combinatorial Algorithms

### Freedom SDK for Metal

**Bare metal software**
- C Runtime
- CSR / MMIO + drivers
- FreeRTOS kernel
- Example programs
- Industry standard benchmarks

### Freedom SDK for Linux

**Embedded Linux software**
- Yocto / OpenEmbedded based
- Includes U-Boot and OpenSBI
- Virtualization (AIA, IOMMU, KVM)
- Enhanced perf support
- Enhancement kernel for IP
- Power management support

### Models

**Simulation models**
- Cycle model
- Fast functional model
- SystemC interface
- TLM 2.0 interface
- Single or Multi-threaded
Empowering innovators

www.sifive.com