RISC-V: Potentials of open computing for Europe

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TUM Venture Labs, 23 April 2024

About Me

Professor at Hochschule München University of Applied Sciences
Computer Architecture, Embedded System Security

Member of the RISC-V board of directors
Representing the individual community members

Director at Free and Open Source Silicon Foundation
Advocacy, guidance and events

01

What is RISC-V?

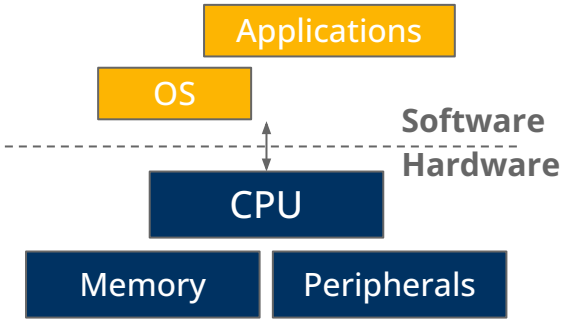
RISC-V is an Open Instruction Set Architecture

Instruction Set Architecture (ISA)
Interface between Software and Hardware (CPU)

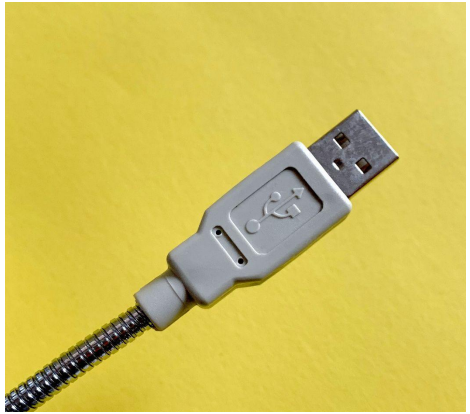
ISAs don't matter
Companies differentiate on products, small part of system

ISAs matter
High software porting costs and effort

ISA defines instructions and conventions
From baseline integer arithmetics, over privileged instruction to complex vector processing

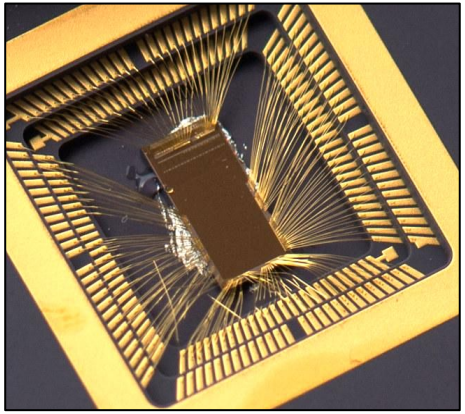


Global standards are a catalyst to accelerate technical innovation



Standards have been critical to technology innovation, adoption, and growth for decades

Standards create access to opportunities and spur growth for a wide range of stakeholders



RISC-V is a standards-defined Instruction Set Architecture developed by a global community

02

RISC-V Standard

RISC-V Organization

RISC-V International
Global nonprofit association based in Switzerland

Over 350 industry members from over 70 countries
Across industries and technical disciplines

Development of the RISC-V standards
Large number of Technical Working Groups

Device certification

Ecosystem & community support

RISC-V Base Instruction Set and Modularity

RISC-V is a modular instruction set architecture

- Baseline instruction set with ~45 instructions
- Even privileged spec is separate
- Large set of standardized extensions
- Greenfield opcode-space for custom extensions

Thereby, RISC-V allows for great flexibility

- Spans large space of CPU microarchitectures (deeply embedded to HPC)
- System designers can pick extensions to their needs and extend

Fragmentation versus diversity

Fragmentation
Same thing done different ways

Diversity
Solving different problems

Managing Diversity for RISC-V

Raw extensions

- Base + standard extensions + custom extensions
- Full suite of options for experimentation and specialized uses
- Massive combinatorial space of options

ISA Profiles

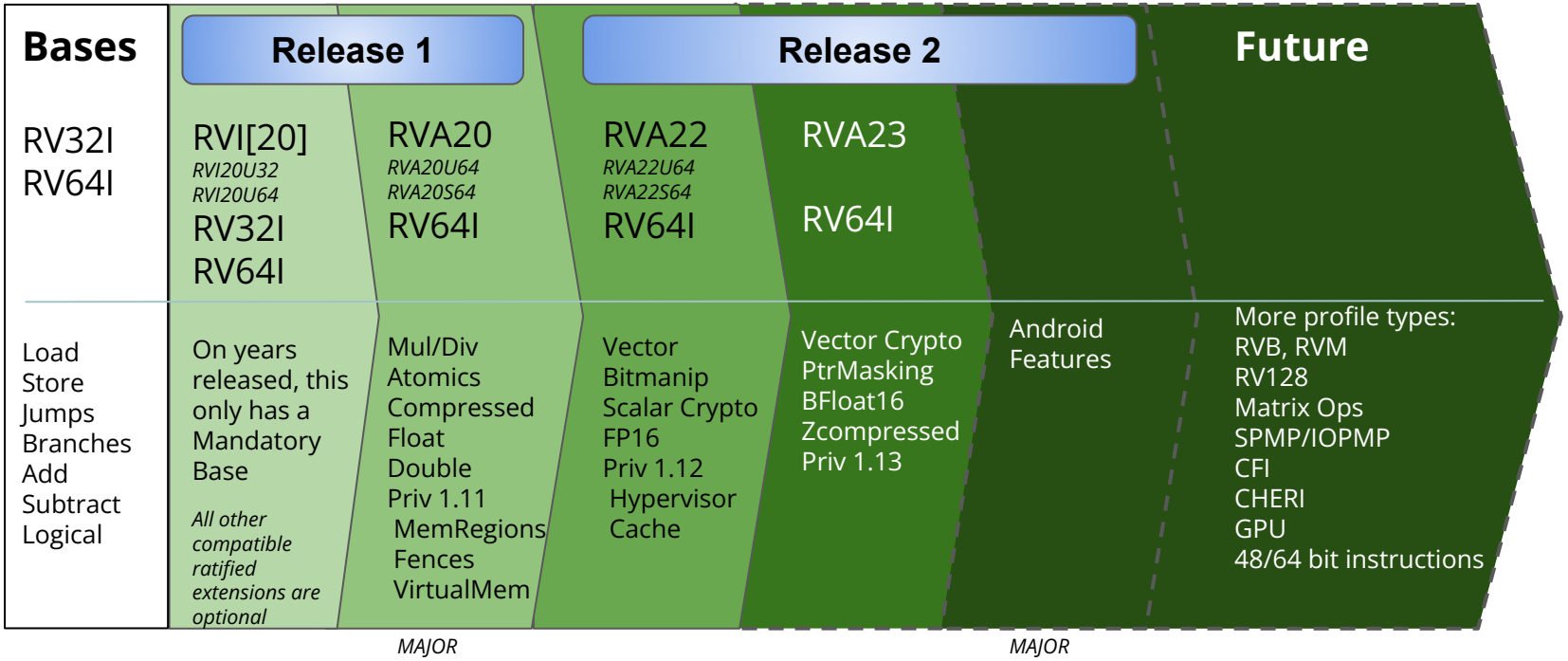
- Packages of ISA extensions for given domain
- Initial set: RVI20 (basic), RVA20/22/23 (application processor)
- Factor out common ISA combinations for use in platform standards

Platform standards

- Hardware/software standards for platforms (much more than just ISA)
- Initial focus OS-A platform for Unix-like OS (includes IOMMU, AIA, etc)

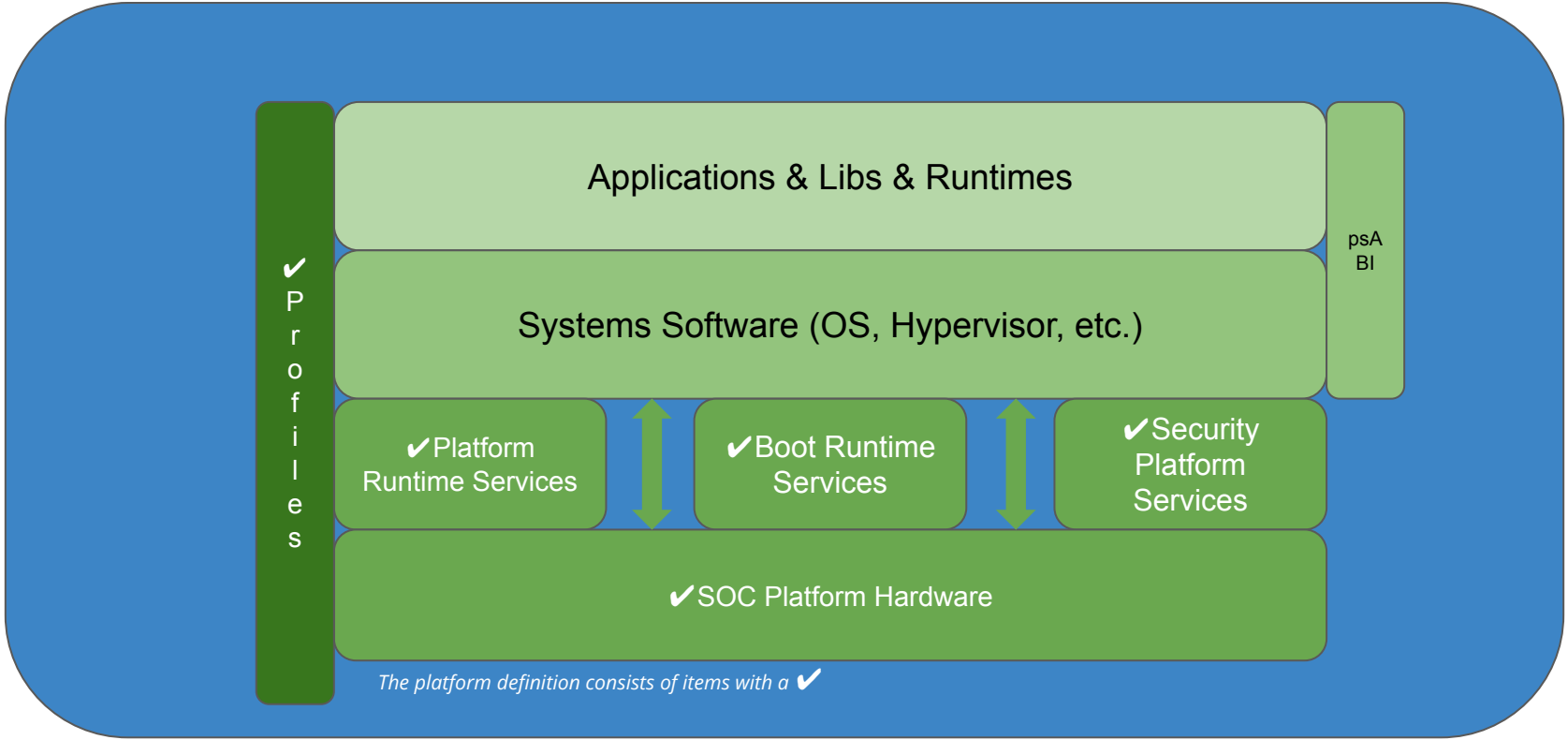
Diversity: Solving different problems

Profiles



- *Only a subset of extensions are listed above and it is not an exhaustive list*
- *Some extensions may be optional or non-profile in one profile and be mandatory in another*

Platforms

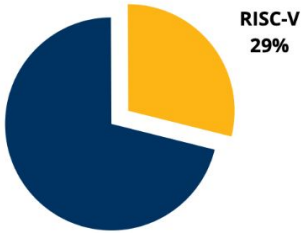

✔Profiles
Applications & Libs & Runtimes
Systems Software (OS, Hypervisor, etc.)
psA
BI
✔Platform Runtime Services
✔Boot Runtime Services
✔Security Platform Services
✔SOC Platform Hardware
The platform definition consists of items with a ✔

03

RISC-V Traction

Selected Market Share Projections for RISC-V in 2030

Wearables
MCU

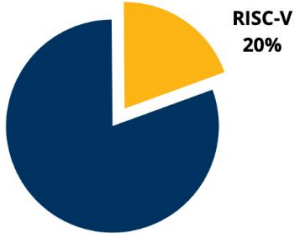


TAM: 2.6B units

Computing
Notebooks

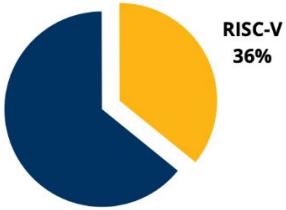
TAM: 2.7B units

Communications
5G Infrastructure



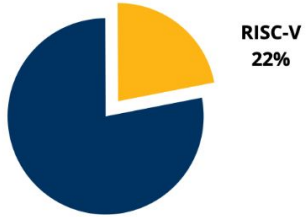
TAM: 1.8B units

Consumer
AI Acceleration



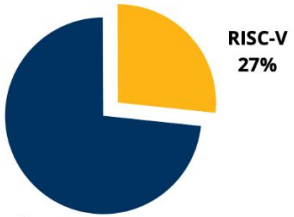
TAM: 6.4B units

Industrial
Smart Grid



TAM: 670M units

Automotive
AI Acceleration



TAM: 260M units

Source: The SHD Group, November, 2023

Based on projected SoC volumes

the SHDgroup

New RISC-V processors

Codasip

Codasip first commercial CHERI security implementation

semidynamics
silicon design and verification services

RISC-V Tensor Unit for ultra-fast AI solutions

SiFive

Performance P870 and Intelligence X390 for generative AI and ML

VENTANA

Data center CPU chiplet solution with I/O hub, DDR memory, PCIe, up to 192 cores

芯来科技 NUCLEI

NA900 certified compliant ASIL D of ISO 26262 standard

Tiempo SECURE

TESIC RISC-V IP passes SERMA CC EAL5+ security tests

CAST

BA5x™ RISC-V processors for low power and EMSA5-FS for functional safety

ICT

Use of AI to design RISC-V CPU in under 5 hours

Applications

Qualcomm RISC-V wearable platform with Google Wear OS

First generative AI RISC-V appliance

RISC-V tablet, portable Linux console, and cluster

Vega, the first RISC-V 10 gigabit Ethernet switch

First RISC-V IoT security Towngas Chip has sold over 1,000,000 units

Two self-developed RISC-V communications chips

Andes N25F for performance and low power in enterprise SSD controller, AndesCore™ RISC-V multicore vector processor

MTIA v1: Meta's first generation AI inference accelerator

Developing Ecosystem

THE LINUX FOUNDATION PROJECTS

RISE

RISE
RISC-V Software Ecosystem

Accelerating the RISC-V Software Ecosystem

The RISC-V Software Ecosystem (RISE) project is a collaborative effort led by industry leaders with a mission to accelerate the development of open source software for the RISC-V architecture.

QUINTAURIS

Quintauris is advancing the adoption of RISC-V globally by enabling next-generation hardware development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JUNE 24 – 28 | MUNICH 2024
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RISC-V shapes the future of semiconductors!
https://riscv-europe.org/summit/2024

Thank you!

#RISCVEVERYWHERE

Do you have any questions?

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